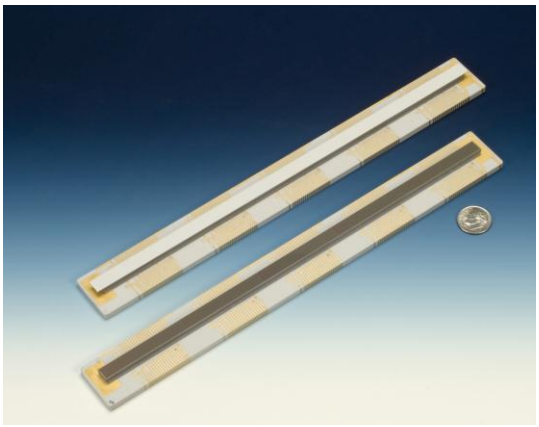
Fairchild Imaging CCD 5023

PRODUCT DESCRIPTION

The CCD 5023 is a high sensitivity Time Delay Integration (TDI) CCD sensor designed for wide area scanning operations such as dental or medical x-ray imaging. It has the following operational advantages: Vertical summing stage allows up to three (binning 3 x 3 case) vertical shifts of charges during a line time.



The vertical registers operate in 4-phase mode.

A readout register including 1,734 stages multiplexes the charges of each column with 1,704 stages allowing receiving charges from the 1,704 useful columns and 15 stages as prescan elements on each side. The register is designed to store and to transfer up to 5 times the charge given by a pixel of 27µm x 27µm.

This horizontal register operates in two-phase mode.

Vertical CCD registers (TDI registers or columns) may operate in inverted mode (MPP: Multi Phase Pinned). Horizontal shift register can operate in the inverted mode.

An output amplifier is located at the end of the readout register. This output amplifier consists of a reset transistor and a dual stage source follower.

The CCD chip is buttable on two sides. The chip design is produces a dead zone between two-butted CCD of less than 100µm.

FEATURES

CCD technology

TDI mode and full frame mode operation

Multiple chips assembled on a ceramic package

Fiber optic faceplate

Scintillator layer

Plastic lid

Available in two versions:

- Version P: 3 die version for panoramic applications
- Version C: 5 die version for cephalometric applications

Available in two versions:

- 242 lines x 1704 pixels
- Pixel dimensions are: 27µm x 27µm
- Dimensions of the image are 6.53mm x 46.0mm

On-chip binning capability

Architecture Features of One Die

PARAMETER	SPECIFICATION	UNIT	NOTES
Pixel size	27 x 27	µm x µm	
Optical pixel aperture	100	%	(1)
Reduced Optical pixel aperture			
typically	90	%	
max. limits	± 4	%	
Number of photosensitive pixels on one line in image area		-	
	1,704	-	
Number of photosensitive lines in image area		-	
	242	-	
Total image area	46.0 x 6.528	mm x mm	
Number of readout registers	1	-	
Number of readout register stages	1,734	-	(2)
Number of prescan elements	15	-	
Number of postscan elements	15	-	
MPP technology	Yes	-	
Pixel clocking scheme, vertical (TDI)	4 phases	-	
Readout register clocking scheme, horizontal	2 phases	-	

NOTES:
(1) 286 pixel columns have reduced optical aperture of 86 - 94%
(2) Including 15 pre- and 15 post-scan elements

SENSOR ASSEMBLY

CCD Chips Assembly

PARAMETER	SPECIFICATION			UNIT
	MIN	TYP	MAX	
Total sensitive length				
Version P	-	138	-	mm
Version C	-	230	-	mm
Total sensitive width	-	6.528	-	mm
Blind gap between two butted chips	-	-	100	µm
Pixel alignment accuracy in column (vertical) direction in butted zone	- 50	0	+ 50	µm

X-RAY OPTICS
In order to convert X-rays into light detectable by the CCD, a scintillator is optically coupled to the CCDs.
The optical stack is the following, when seen from the X-ray source :
1. Scintillating layer
2. Fiber optics (about 3mm thick)
3. CCD

TYPES OF SCINTILLATOR
Type of scintillator is for Version P and C Standard Kodak Lanex® Regular with standard thickness manufactured after 1999.

PLASTIC LID
A plastic cover is glued (dust-tight and light-tight) on the ceramic to protect the CCD and the scintillator. The thickness of the lid is decreased in front of the active area, to minimize X-ray absorption in the lid.

ELECTRICAL INTERFACE
Principle: The sensors use a ceramic plate: the electrical connection can be made by pressing the sensor against a PCB through an anisotropic conductive film. For each connection, the contact area goes all the way around the ceramic plate.

Contact Area Identification: When seen from the contact side, the numbering of the contacts starts near the mark at the corner of the ceramic plate.

Contact #	Symbol	Function
1	R	Output diode reset clock
2	VRD	Output diode reset drain
3	VSRC	Output amplifier source supply
4	VOUT	Video output signal
5	VDD	OUTPUT AMPLIFIER DRAIN SUPPLY
6	VOG	Register output gate bias
7	VSS	CCD substrate bias.
8	HSG	Readout register horizontal summing gate clock
9	VD	Drain bias
10	V3	CCD vertical TDI transfer clock 3
11	V2	CCD vertical TDI transfer clock 2
12	H1	CCD readout register clock 1
13	VS2	Summing well clock in vertical direction 2
14	H2	CCD readout register clock 2
15	VS3	Summing well clock in vertical direction 3
16	V1	CCD vertical TDI transfer clock 1
17	V4	CCD vertical TDI transfer clock 4
18	VTG	Vertical transfer gate between vertical summing well and readout register.
19	VS1	Summing well clock in vertical direction 1
20	-	Reserved, contact need not to be implemented
21	VSS	CCD substrate bias.
22	-	Reserved, contact need not to be implemented
23	-	Reserved, contact need not to be implemented
24	-	Reserved, contact need not to be implemented
25	-	Reserved, contact need not to be implemented
26	-	Reserved, contact need not to be implemented
27	-	Reserved, contact need not to be implemented
28	Test1	Alignment test track 1
29	Test2	Alignment test track 2

Electrical Alignment Test

In order to facilitate the testing of good alignment of the sensor on the PCB while assembly, a special pattern is needed on the ceramic plate. It consists of two conductive tracks that are short-circuited, to test that minimum half of the width of the tracks are in contact with the PCB pad.

The electrical alignment test pattern is next to contact number 27 (see fig. 1a and 1b, detail X).

Mechanical Interface

The drawings below show the external dimensions of the sensors as well as the positioning of the contact areas.

Two sides of the ceramic plate should be usable as mechanical reference. A triangle mark on the ceramic plates shows the corner of the reference sides (see figure 1a and1b).

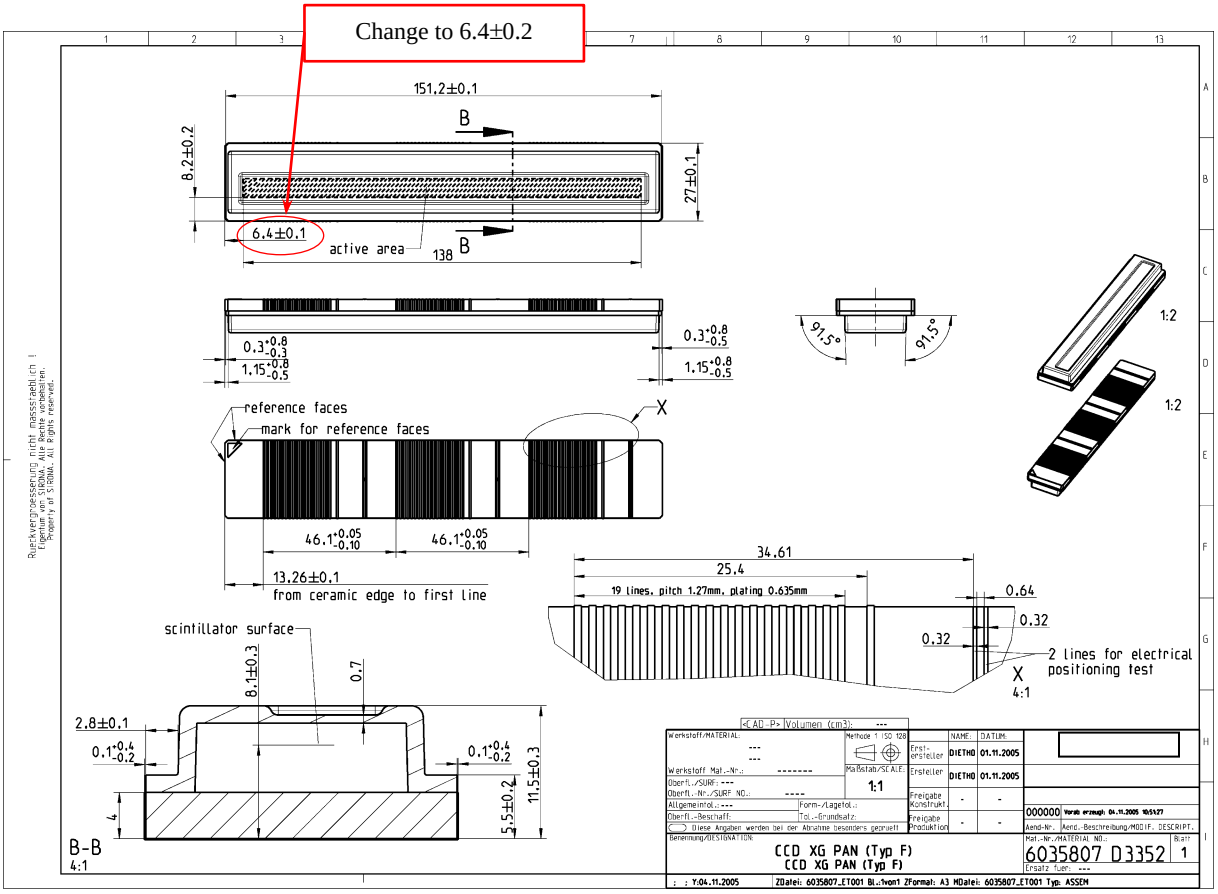


Figure 1a: Sensor outline pan version

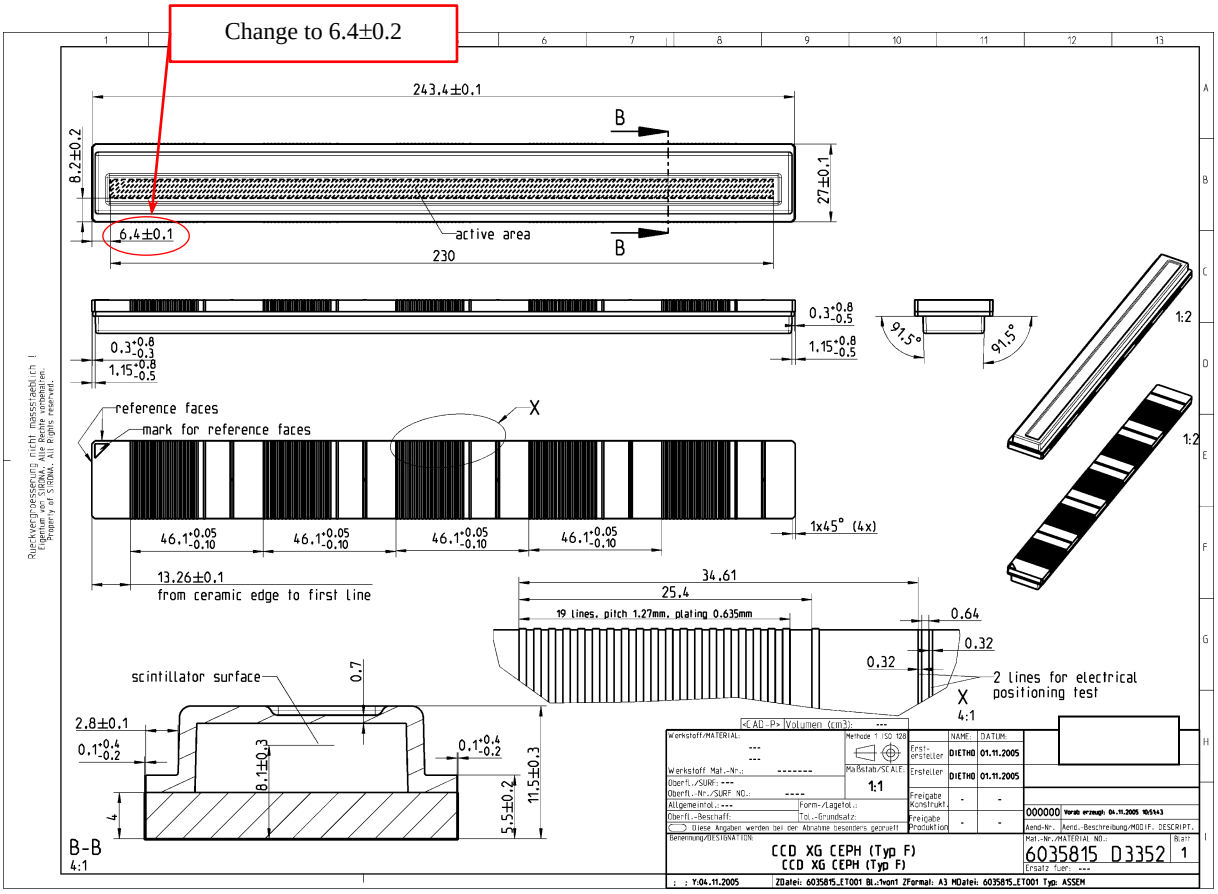


Figure 1b: Sensor outline ceph version

The numbering of the contacts starts near the mark at the corner of the ceramic plate seen from the plastic lid side. Drawing shows situation for pan type, ceph type is equivalent.

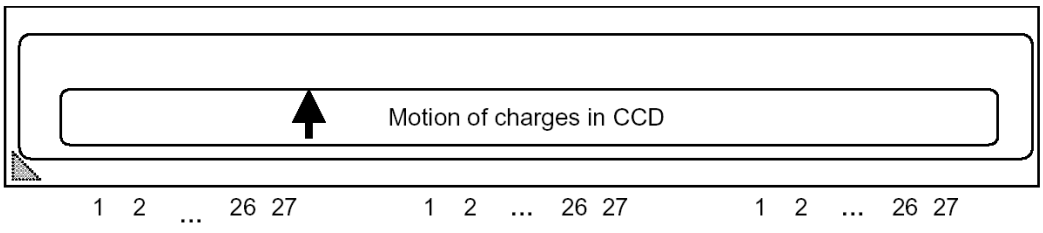


Figure 1c: Numbering and motion of charges

Operating Frequencies

PARAMETER	SPECIFICATION			UNIT
	MIN	TYP	MAX	
TDI speed	-	21.6	44	mm/sec
Line rate		800 Hz		
Vertical transfer time (27µm pixel)	22	28	-	µs
Horizontal register transfer frequency	-	1.5	3	MHz

Table 3: CCD operating frequencies without binning

DC Operating Voltages

PARAMETER	SYMBOL	VALUE			UNIT
		Min	TYP.	Max	
Potential reference, CCD substrate bias, connected to die attach area of package.	VSS	0	0	0	V
Drain bias	VD	14.5	15	15.5	V
Readout output gate bias	VOG	0	0	0	V
Output amplifier drain supply	VDD	14.5	15.0	15.5	V
Output amplifier source supply	VSRC	0	0	0	V
Output diode reset bias	VRD	14.5	15.0	15.5	V

Table 4: CCD DC voltages

AC Operating Voltages

PARAMETER	SYMBOL	VALUE			UNIT	NOTES
		MIN	TYP	MAX		
Vertical register transfer clocks: (MPP wells)	V2, V3, V4					
- Low level :		- 9.5	- 9	- 8.5	V	
- High level :		2.5	3	3.5	V	
Vertical register transfer clock 1 (MPP-barrier):	V1					
- Low level :		- 9.5	- 9	- 8.5	V	
- High level :		5.5	6	6.5	V	
Vertical register summing well clock :	VS1					
- Low level : - High level :		- 9.5	-9	- 8.5	V	
		2.5	3	3.5	V	
Vertical register summing well clocks:	VS2, VS3					
- Low level :		- 3.5	-3	- 2.5	V	
- High level :		6.5	7	7.5	V	
Summing well to readout register transfer clock :	VTG					
- Low level :		- 9.5	- 9	- 8.5		
- High level :		2.5	3	3.5	V	
					V	
Readout register clocks :	H1, H2					
- Low level :		- 3.5	-3	- 2.5	V	
- High level :		6.5	7	7.5	V	
Readout register summing gate clock	HSG					
- Low level :		- 3.5	- 3	- 2.5	V	
- High level :		6.5	7	7.5	V	
Output diode reset clock :	R					
- Low level :		0	0.3	0.5	V	
- High level :		11.5	12	12.5	V	

Table 5: AC Voltages

ELECTRO-OPTICAL PERFORMANCE

Clock Capacitance

Parameter		Specification TYP	Unit
Image area gate capacitance	V1-V4	20	nF
Vertical summing gate capacitance	VS1 - VS3	240	pF
VTG		380	pF
Horizontal gate capacitance	H1-H2	1 000	pF
Summing well gate capacitance	HSG	260	pF
Reset gate capacitance	R	50	pF

Electrical Characteristics

Pixel: 81 µm x 81 µm (Binning 3x3) in full frame mode, unless otherwise specified.

PARAMETER	SPECIFICATION MIN	TYP	MAX	UNIT	NOTES
DC output voltage	10.0	11.5	12.5	Volts	
Supply current (static) on VDD per amplifier	-	1.7	6.0	mA	(1)
Output amplifier impedance	300	650	900	Ω	
Pixel saturation charge : 27 µm x 27 µm :	800	900	-	Ke-	
Saturation charge of readout register	2.4	2.8	-	Me-	(5)
Saturation charge of horizontal summing gate	2.4	2.8	-	Me-	(5)
Conversion factor absolute min-max range	1.5	1.7	1.95	µV / e-	
Output voltage			6.0	V	(4)
Transfer efficiency along vertical register (image area)	0.99995	-	-	-	(2)
Transfer efficiency along readout register	0.99995	-	-	-	(2)
RMS total noise in darkness	-	150	200	µV	
Dynamic range (Vsat / output noise)	10 000	-	-	-	
Linearity error	-	-	+-2	%	(3)

1. At + 25 °C
2. By stage of 27 µm, at Vsat/2
3. From 10% to 95% of saturation (Saturation level is reached, when the output signal differs ± 10% from the regression line)
4. At 4x1 binning and actual conversion factor
5. May be tested in 4x1 or 5x1 binning mode.

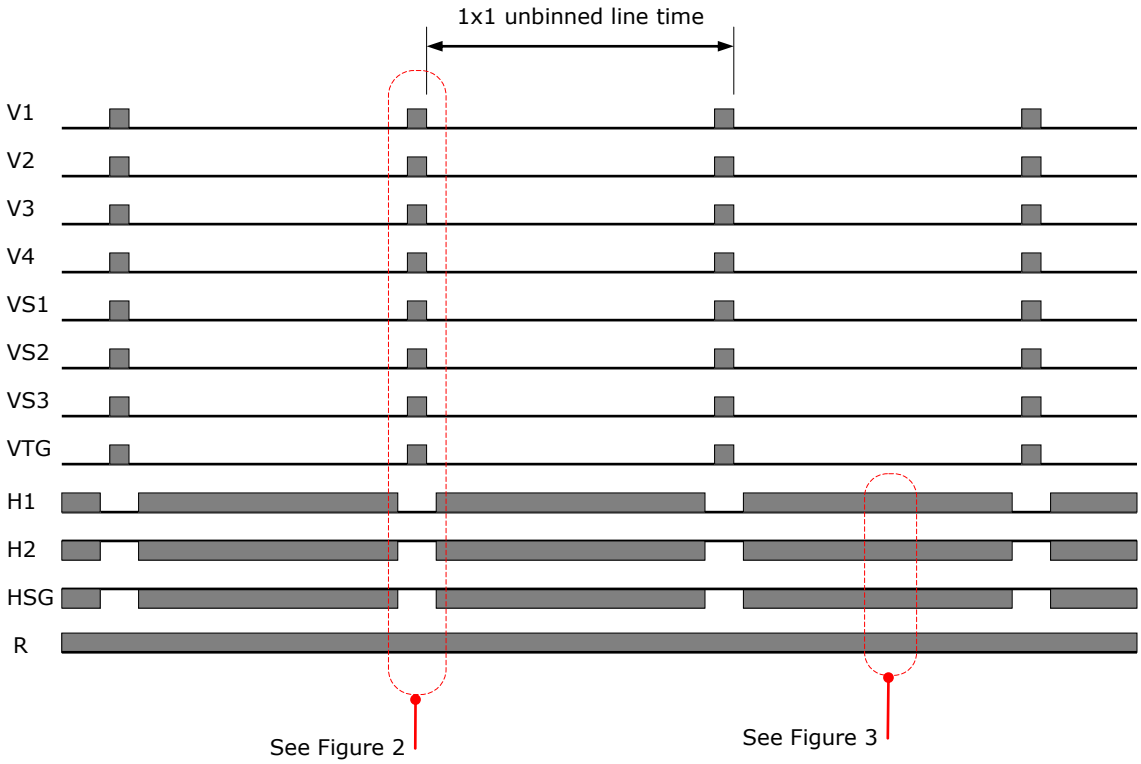


Figure 1: General TDI timing, 1x1 mode without binning

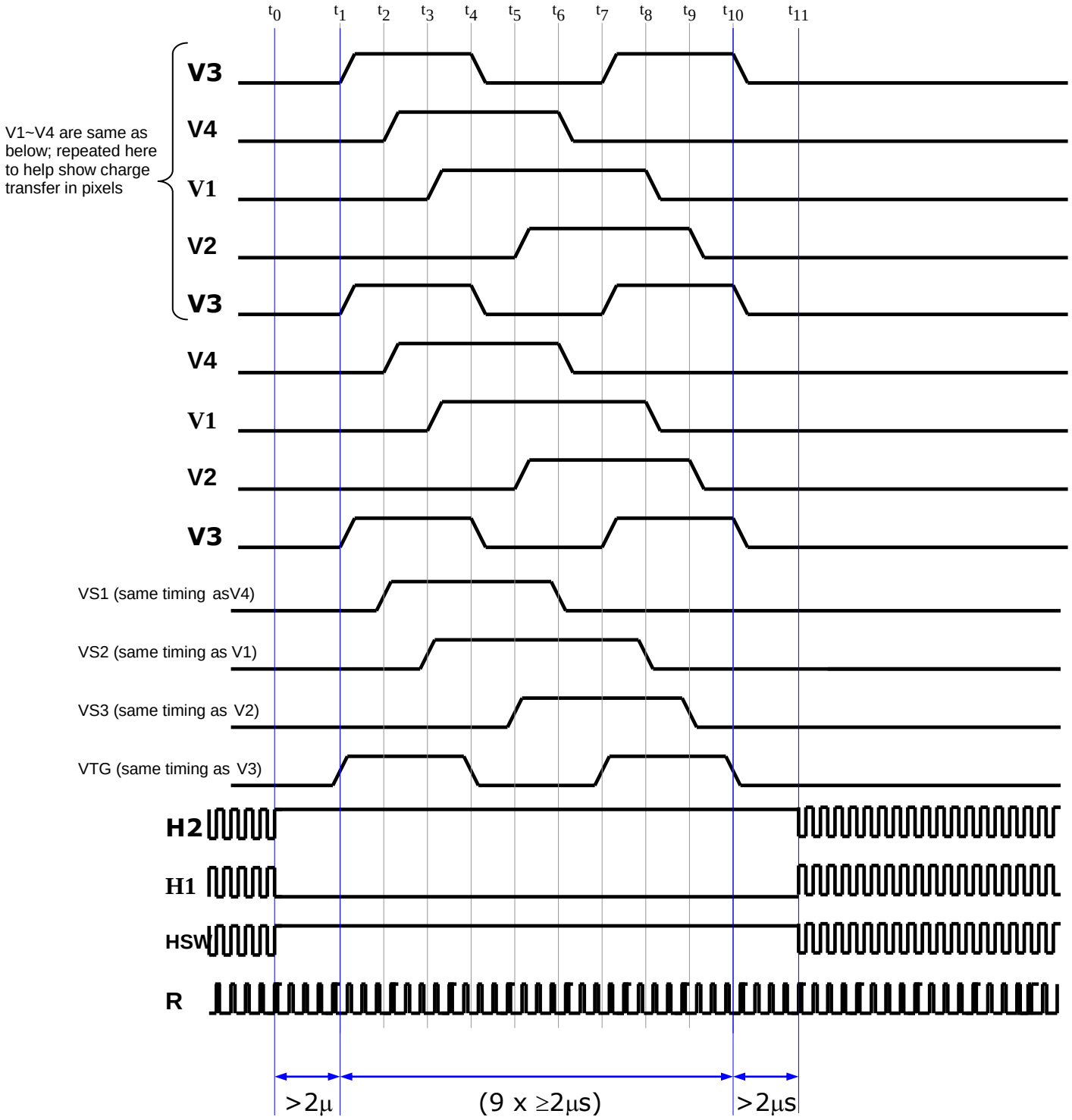
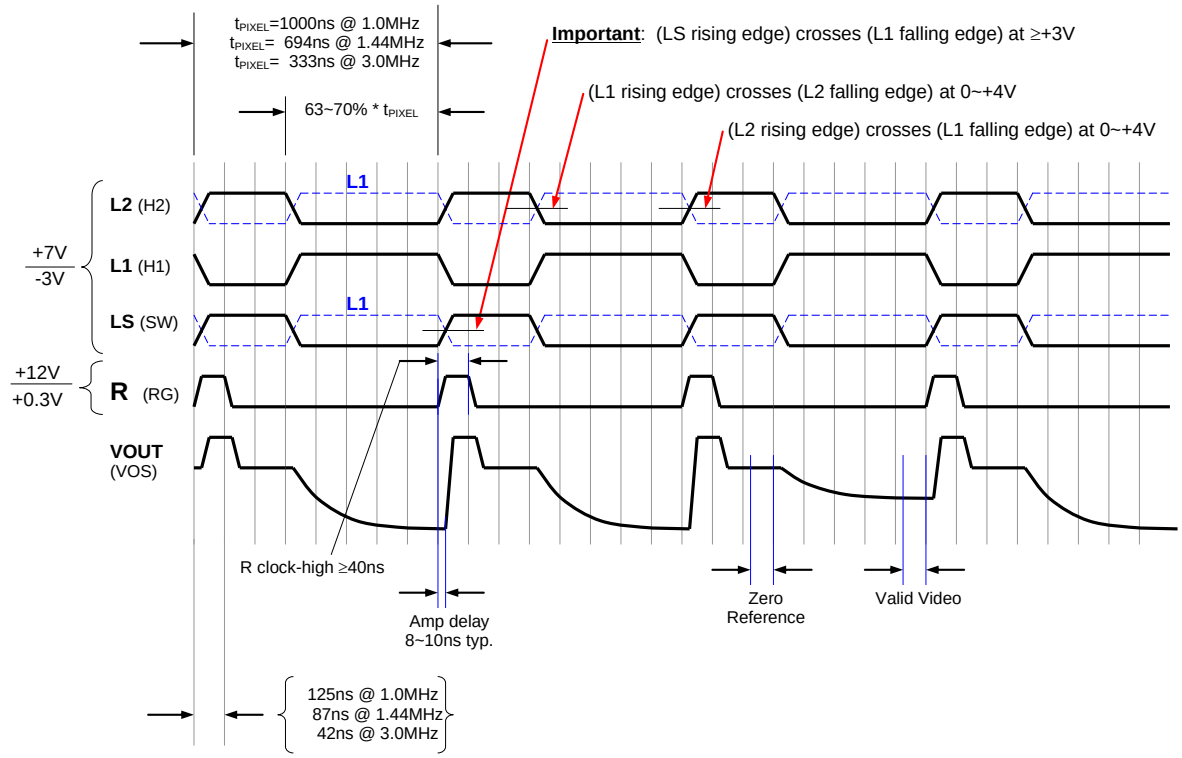


Figure 2: Vertical transfer timing for 1x1 unbinned mode



Slopes for H1, H2 (between 10% and 90% of amplitude): >60ns
Slopes for HSG, R (between 10% and 90% of amplitude): >40ns

Figure 3A: CCD5023 Horizontal Transfer Timing (TDI Without Binning): Pixel Readout Detail View

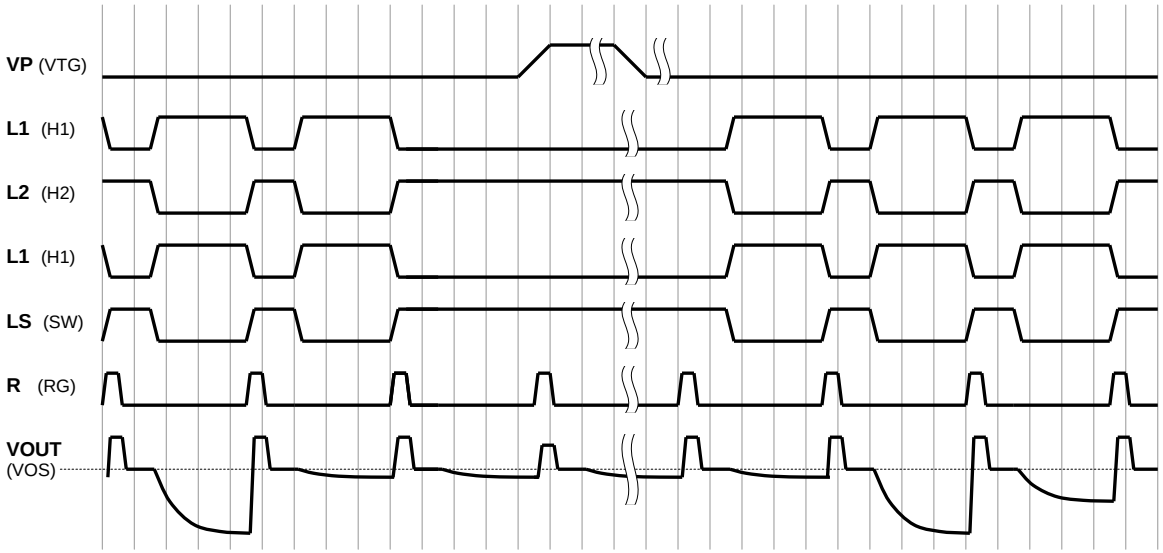


Figure 3B: CCD5023 Horizontal Transfer Timing (TDI Without Binning): During Vertical to Horizontal Transfer

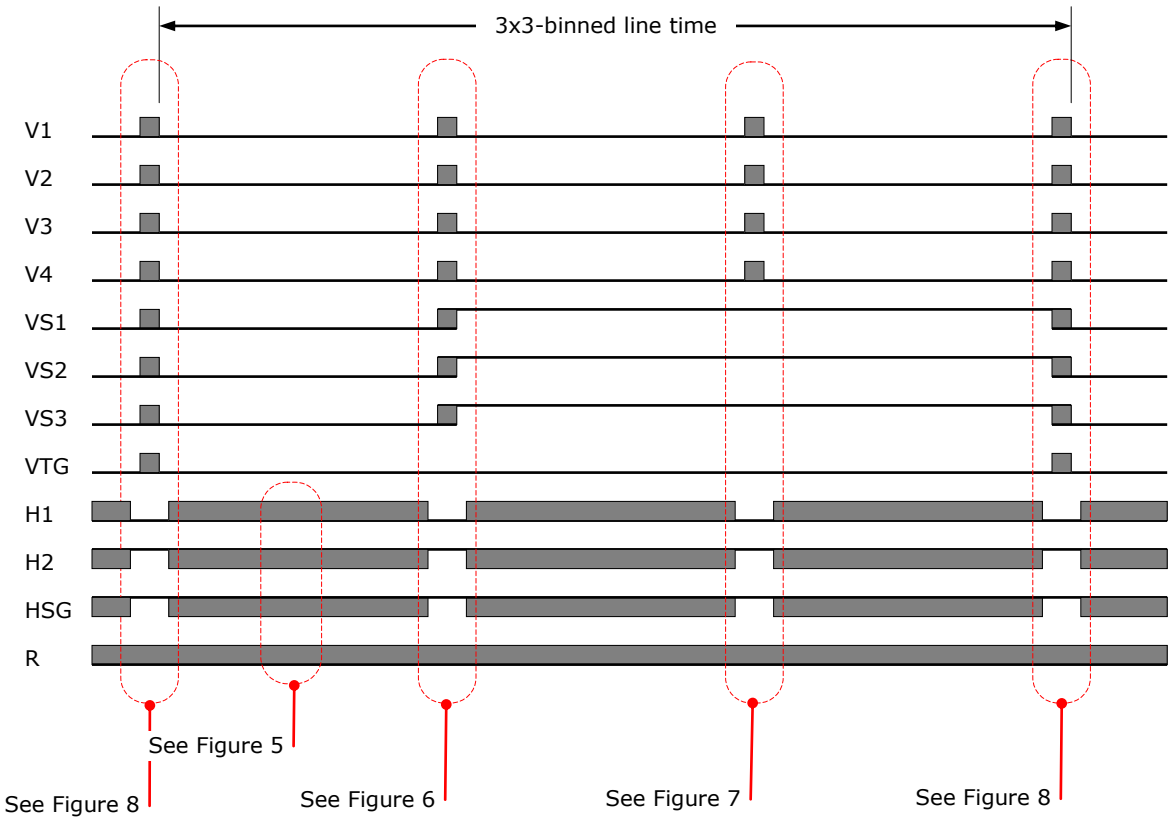


Figure 4-1: General TDI timing with 3x3 binning

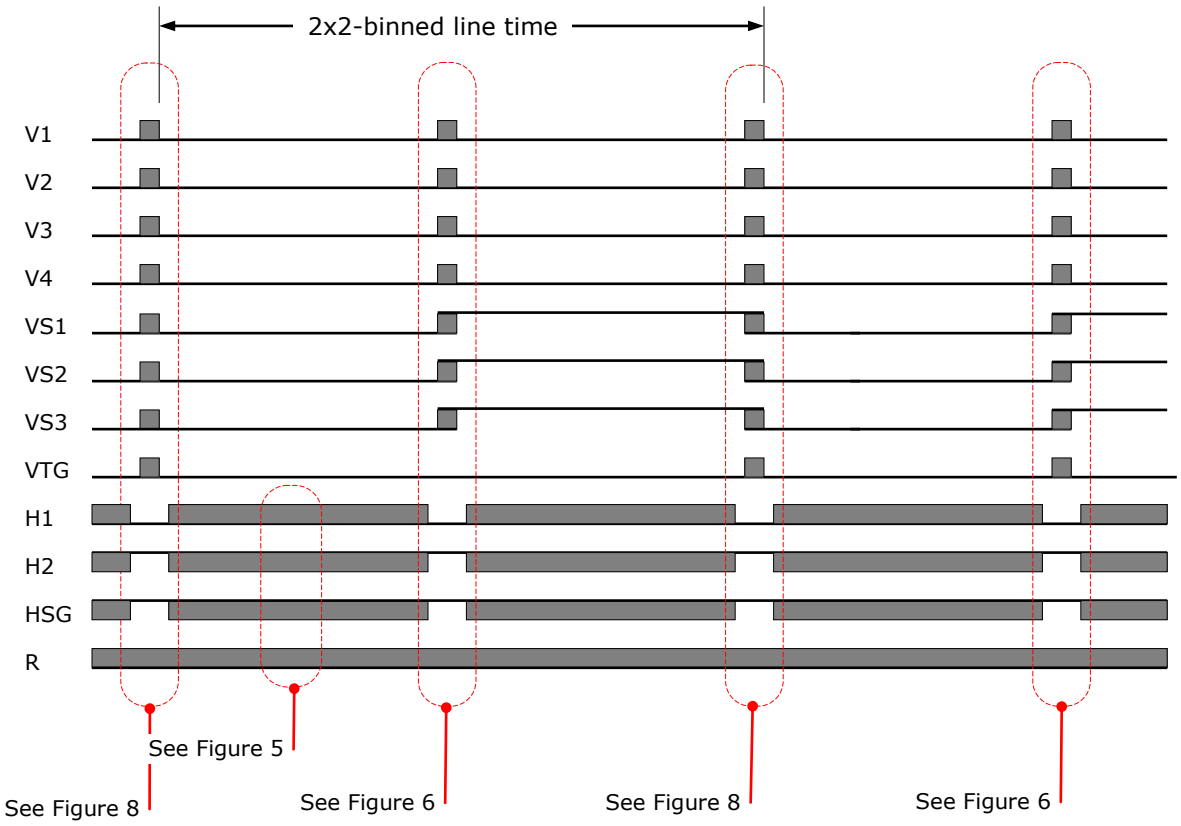


Figure 4-2: General TDI timing with 2x2 binning

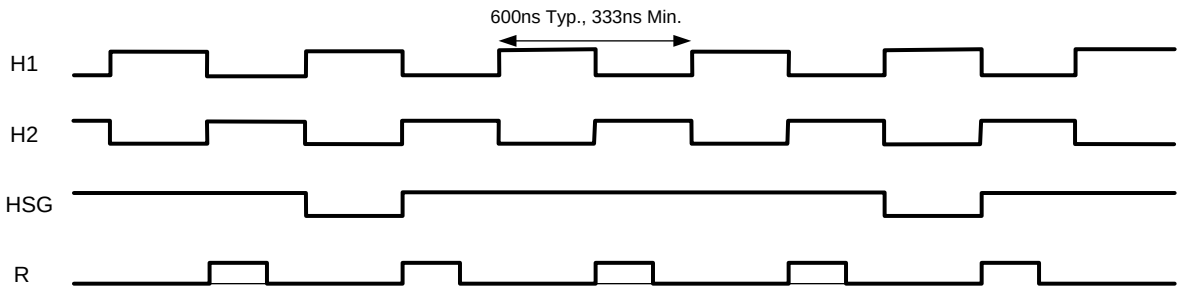


Figure 5: Horizontal transfer timing,
TDI with 3x3 bining

- Slopes for H1, H2 (between 10% and 90% of amplitude): > 60ns
- Slopes for HSG, V (between 10% and 90% of amplitude): > 40ns

15 prescan stages (including HSG stage) = 15 at each end of the register

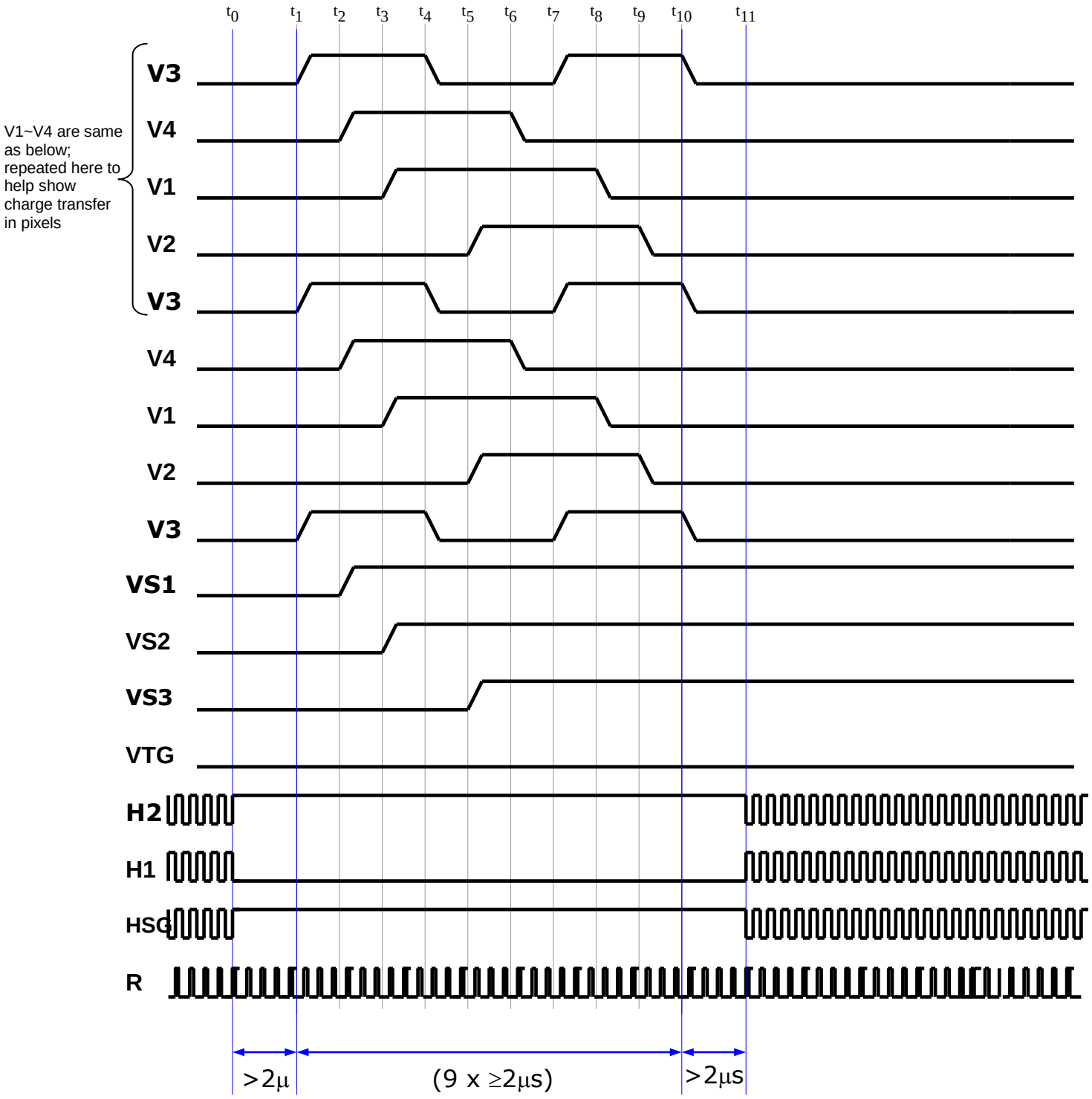


Figure 6: TDI timing with binning: First vertical transfer in binned line

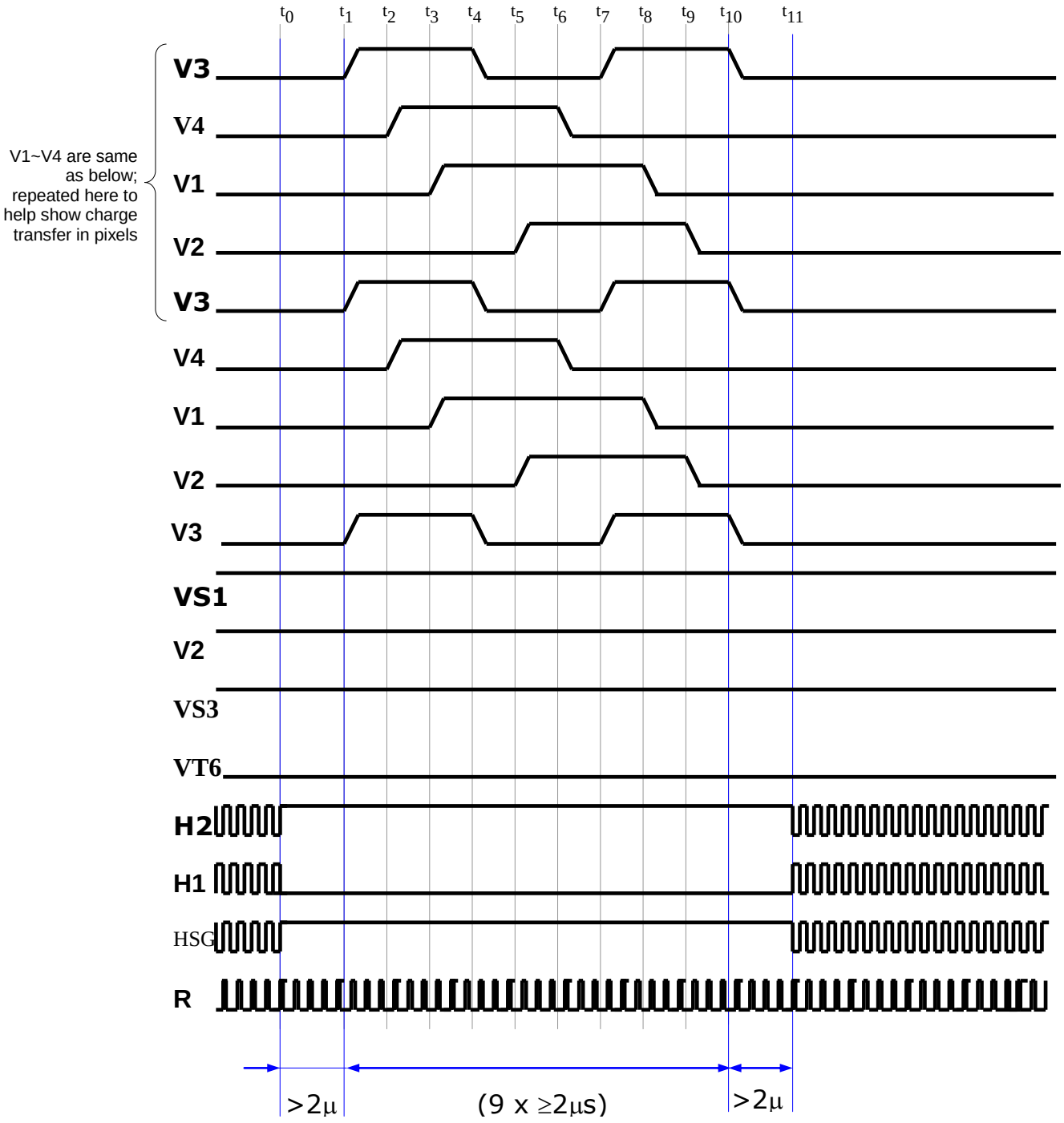


Figure 7: TDI timing with binning: Middle vertical transfer(s) in binned line

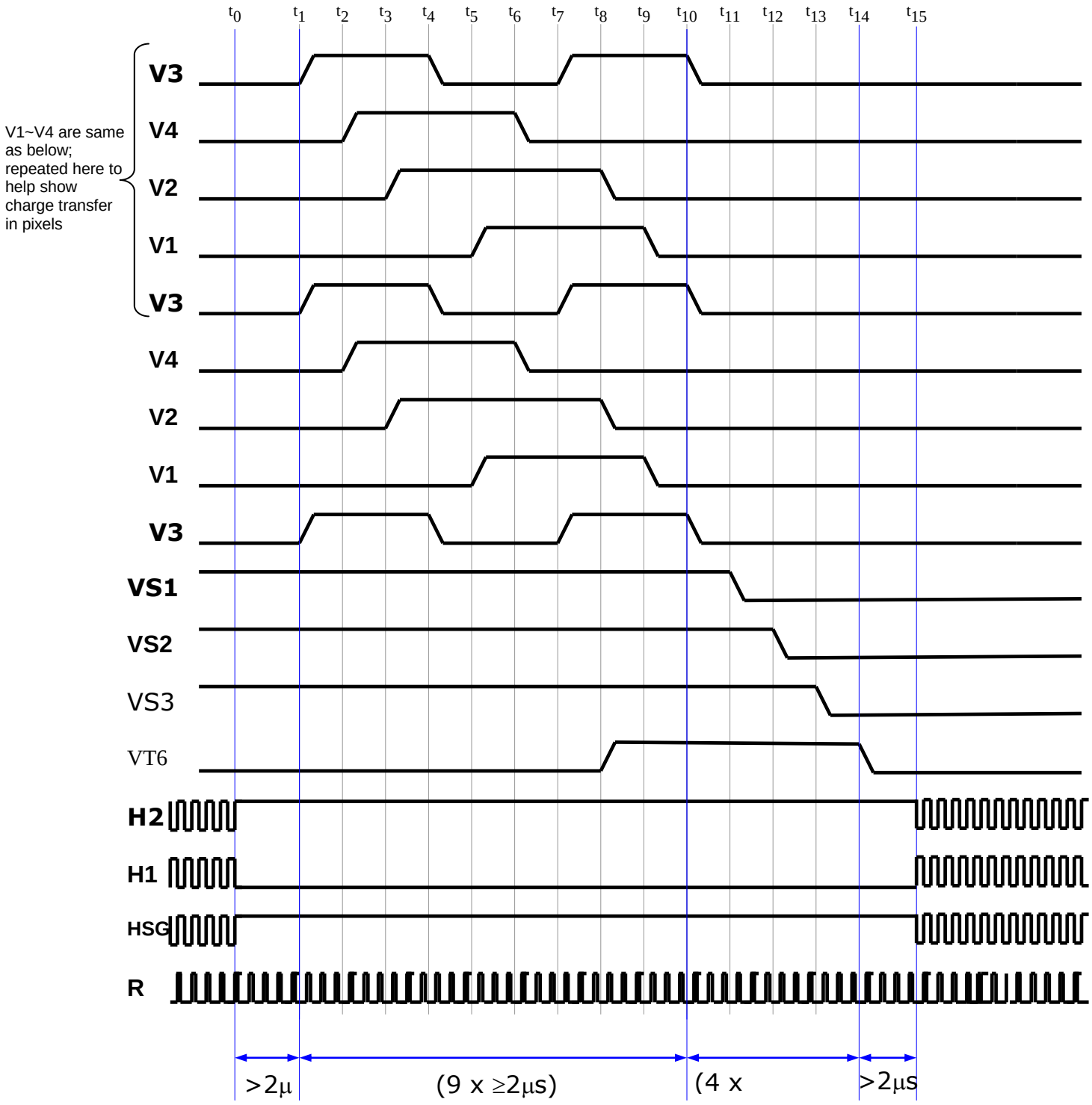


Figure 8: TDI timing with binning: Last vertical transfer in binned line

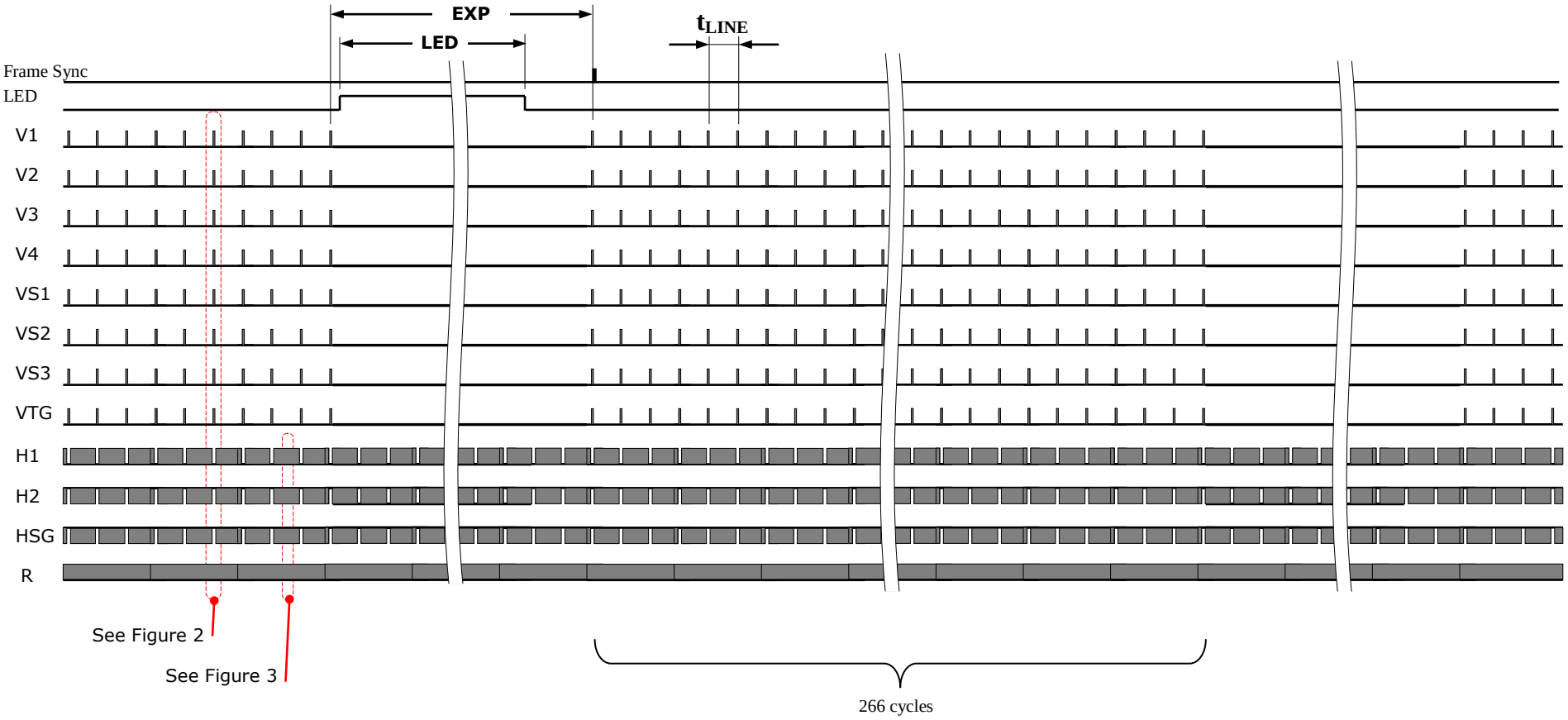


Figure 9: General Full-Frame (FF) timing, 1x1 mode without binning *(used only for engineering test)*

WARRANTY AND CERTIFICATION

Within twelve months of delivery to the original customer, BAE Systems Imaging Solutions will repair or replace, at our option, any Fairchild Imaging components or camera products, if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

BAE Systems Imaging Solutions certifies that its Fairchild Imaging products are fully inspected and tested prior to shipment, and that they conform to the stated specifications.

FOR MORE INFORMATION, CONTACT:

BAE Systems Imaging Solutions
1801 McCarthy Blvd.
Milpitas, CA 95035 USA
Telephone 800 325 6975
Fax 408 435 7352
www.fairchildimaging.com

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