Low FPN High Gain Capacitive Transimpedance Amplifier for Low Noise CMOS Image Sensors

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ABSTRACT

In this paper we introduce a low fixed pattern noise (LFPN) capacitive transimpedance amplifier (CTIA) for active pixel CMOS image sensors (APS) with high switchable gain and low read noise. The LFPN CTIA APS uses a switched capacitor voltage divider feedback circuit to achieve high sensitivity, low gain FPN, and low read noise. This paper discusses the operation of the LFPN CTIA APS, and presents a theoretical analysis of its gain FPN and read noise. We do not analyze the effect of 1/f noise, since it is typically much smaller than the thermal and shot noise effects. Monte Carlo simulation of gain FPN and SPICE simulation of read noise are also presented. For a 0.35μm CMOS LFPN CTIA at room temperature and an output data rate of 16Mpixel/sec, we show that the pixel amplifier gain FPN is less than 0.0064, where FPN is defined as the ratio of standard deviation to mean. The read noise and dynamic range are less than 3 electrons RMS and greater than 90dB respectively. We find that theory and simulated results match closely.

Keywords: CTIA, FPN, Read noise, CMOS image sensors, APS.

1. INTRODUCTION

CMOS image sensors are beginning to compete with CCDs in the consumer and PC markets, but they are still too noisy and lack the sensitivity of CCDs for most industrial and scientific products. If CMOS image sensors are going to compete with industrial and scientific CCDs, they must further reduce their read noise and increase their sensitivities. In order to achieve this goal, several approaches have been investigated, including photogate APS,[1] pinned photodiode APS,[2,3] and stacked APS sensors.[4] The advantages and disadvantages of these techniques are discussed by Lule.[4] Athough all of these techniques can lead to lower noise and higher sensitivity CMOS image sensors, they still do not achieve the performance levels of scientific CCD image sensors.[5] If the silicon area is available, such as in linear sensors or stacked APS, another promising method of increasing pixel sensitivity and reducing read noise is by using capacitive transimpedance amplifiers.

Capacitive Transimpedance amplifiers (CTIA) have been used in visible MOS image sensors since the early 1970's.[6] Initially CTIAs were used as column amplifiers in passive pixel MOS image sensors,[6–8] but as CMOS technology scaled, CTIAs were also used as pixel level amplifiers in CMOS active pixel sensors (CTIA APS).[9] CTIA APS can be designed to have high charge to voltage conversion ratios and low read noise, but since high gain requires a small effective feedback capacitance, they often suffer from large gain fixed pattern noise (FPN) because of the large relative variation in the size of small feedback capacitors. Due to their high gain and low noise, CTIA APSs promise higher performance than even scientific CCDs, but to achieve this potential, their gain FPN must be reduced to levels comparable to CCDs.[5]

FPN is the fixed variation in output between pixels given a uniform input. In a perfect image sensor, each pixel would have the same output given the same input, but in actual image sensors the output of each sensor is different. FPN does not change as a function of time and can be characterized, assuming a linear pixel response, as a variation in offset and gain at each pixel. Let the pixel response be described by

$$V_{i,j}(t) = G_{i,j}X_{i,j}(t) + O_{i,j}, \tag{1}$$

where $V_{i,j}(t)$ is the voltage output of pixel i,j at time t, $G_{i,j}$ is the gain of pixel i,j, $X_{i,j}(t)$ is the input signal at pixel i,j at time t, and $O_{i,j}$ is the offset of pixel i,j. Gain FPN is the pixel to pixel variation of $G_{i,j}$, and offset

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FPN is the pixel to pixel variation of $O_{i,j}$. We will focus on the gain FPN in this paper and define it as the standard deviation of the pixel gain divided by the mean pixel gain.

In this paper, we introduce a low FPN (LFPN) CTIA APS with high switchable gain and low read noise. The high gain and low read noise are advantages of using a CTIA, and the low FPN was achieved by using a switched capacitor voltage divider feedback circuit. This circuit delivers the low effective feedback capacitance required by a high gain CTIA, using a much larger feedback capacitor with consequently smaller relative variation and thus low FPN. This paper discusses the operation of the LFPN CTIA APS, and presents an analysis of its gain FPN and read noise. We do not analyze the effect of 1/f noise, since it is typically much smaller than the thermal and shot noise effects. Theoretical results are compared with a standard high FPN CTIA APS. In addition, simulated results from a 7 transistor per pixel 0.35μm CMOS implementation are also presented and compared with theory.

The remainder of this paper is organized as follows. Section 2 describes the operation of an LFPN CTIA pixel and presents analysis of its gain FPN and temporal noise. Section 3 presents simulation results for a 7 transistor LFPN CTIA pixel. Finally, in Section 4, we compare theory and simulation and discuss future directions.

2. THEORY

2.1. Circuit Operation

A schematic of the LFPN CTIA pixel is shown in Figure 1. The circuit consists of a transconductance amplifier TA1, a photodiode, a network of feedback capacitors and switches (C1, C2, Cf, M1, M2), and a bit line select transistor M3. WORD is used to select each row of pixels, BIT is the output bus for each column in the sensor, RESET and GAIN are used to reset the pixel and control the pixel gain, and VREF is the pixel bias voltage. The idea behind the circuit is to use capacitive voltage division between C1 and C2 to reduce the effective size of Cf in the feedback loop of the transimpedance amplifier. This allows Cf to be much larger than would otherwise be allowed by the high gain required for the CTIA. A larger value of Cf will be subject to smaller relative variations which then must have a smaller effect on the CTIA performance. Assuming cascode amplification, most of the gain FPN in a CTIA comes from variations in the feedback capacitors; consequently, large capacitors in the feedback loop reduce the gain FPN.

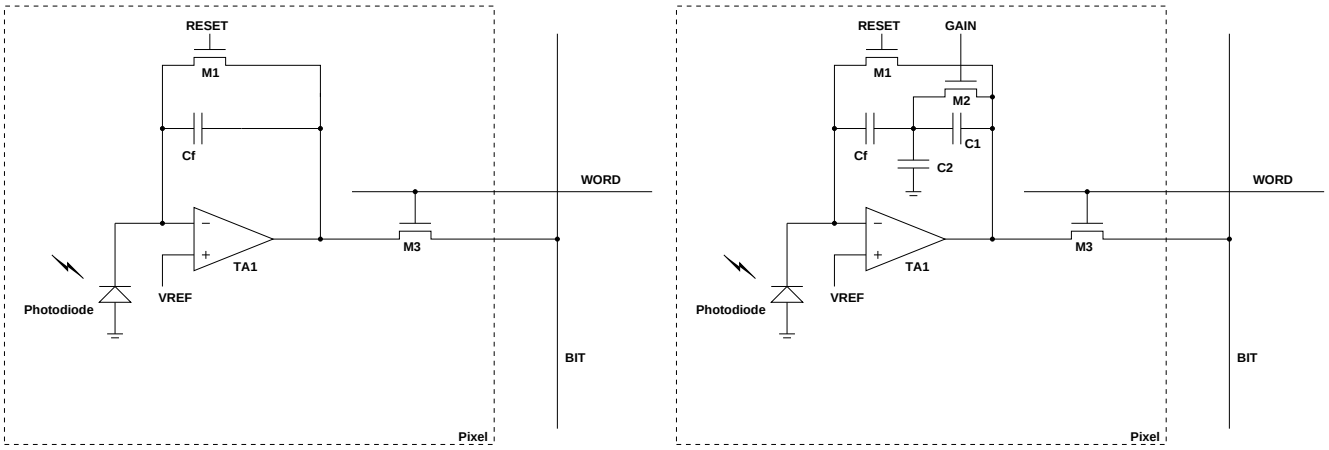

Figure 1. Standard High FPN(left) and LFPN(right) CTIA APS Pixel Schematics

The LFPN CTIA can be operated in either the normal high gain mode or an additional low gain mode. In high gain mode, transistor M2 is switched during reset, allowing the capacitive voltage divider to operate during charge integration. The signal waveforms used for readout and high gain reset are shown in Figure 2. Note that GAIN is pulsed during reset to restore the DC voltage across C2. In low gain mode, transistor M2 is always on, shorting out C1. This reduces the effective pixel gain. Although the circuit looks more similar to a standard high FPN CTIA with M2 on, its gain and FPN are both low in this mode due to the larger value of Cf. The signal waveforms used for readout and low gain reset are shown in Figure 3. After readout and reset are complete, the pixel is ready to start integrating photocurrent.

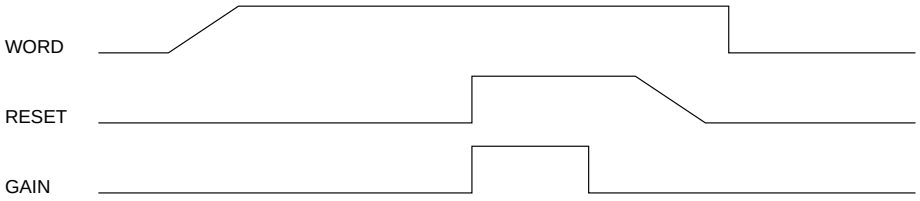

Figure 2. LFPN CTIA Control Waveforms for High Gain Mode

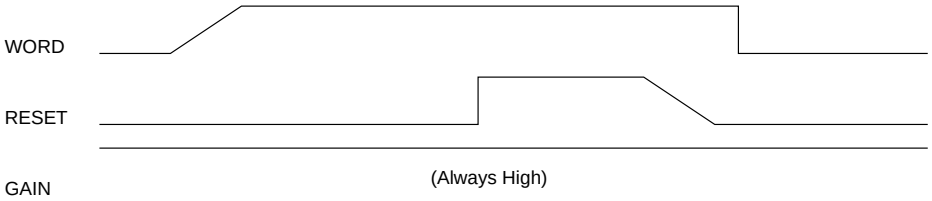

Figure 3. LFPN CTIA Control Waveforms for Low Gain Mode

2.2. Gain Fixed Pattern Noise Analysis

In this section, we analyze the gain FPN of the LFPN CTIA in normal high gain mode and show it to be less than the gain FPN of a standard high FPN CTIA APS. A standard high FPN CTIA APS pixel is also shown in Figure 1. Since we are comparing the two different CTIA circuits, we do not take into account the gain FPN caused by the photodiode. If the gain FPN caused by the CTIA is sufficiently low, the gain FPN of the sensor will be limited by the photodiodes and not by the pixel circuitry.

In each CTIA circuit, the gain FPN depends on the variations in capacitances. In order to characterize this dependence, we will model the value of each capacitor Cx as a uniform random variable C_x. Each such variable C_x used in our analysis has a uniform distribution with a minimum value $\check{c}_x$, a maximum value $\hat{c}_x$, and an average value $\frac{\check{c}_x+\hat{c}_x}{2} = \bar{c}_x$. c_x is a specific value of the random variable C_x. A uniform distribution was selected because the resulting estimated gain FPN will be pessimistic. In addition, we will assume that all capacitances are independent, which is also pessimistic in that it results in a wider gain variance.

Assuming steady state operation, we use the small signal model in Figure 4 to analyze the LFPN CTIA gain FPN in normal high gain mode. Let the effective gain g_{lo} be defined by $g_{lo} = \frac{c_1+c_2+c_f}{c_1 c_f}$. If $\frac{g_m}{g_o} >> c_{pd} g_{lo} + 1$, then it can be shown that the transimpedance of the LFPN CTIA is

$$\frac{v_{o,lo}}{i_{pd}}(s) \approx \left(\frac{1}{s}\right) g_{lo}. \tag{2}$$

Therefore the mean gain is

$$\mu_{g,lo} = \int\int\int g_{lo} p(c_1, c_2, c_f) dc_1 dc_2 dc_f, \tag{3}$$

where $p(c_1, c_2, c_f)$ is the joint probability density function of the uniform random variables C_1, C_2, and C_f. The expected value squared of the gain is given by

$$\sigma^2_{g,lo} + \mu^2_{g,lo} = \int\int\int g^2_{lo} p(c_1, c_2, c_f) dc_1 dc_2 dc_f. \tag{4}$$

Since C_1, C_2, and C_f are uniform, it can be shown that

$$\mu_{g,lo} = \frac{ln(\frac{\hat{c}_f}{\check{c}_f})}{\hat{c}_f - \check{c}_f} + \frac{ln(\frac{\hat{c}_1}{\check{c}_1})}{\hat{c}_1 - \check{c}_1} + \frac{\hat{c}_2 + \check{c}_2}{2} \frac{ln(\frac{\hat{c}_f}{\check{c}_f})}{\hat{c}_f - \check{c}_f} \frac{ln(\frac{\hat{c}_1}{\check{c}_1})}{\hat{c}_1 - \check{c}_1}, \tag{5}$$

and

$$\sigma_{g,lo}^2+\mu_{g,lo}^2 = \frac{1}{\hat{c}_f\check{c}_f}+\frac{1}{\hat{c}_1\check{c}_1}+\frac{\hat{c}_2^2+\hat{c}_2\check{c}_2+\check{c}_2^2}{3}\frac{1}{\hat{c}_f\check{c}_f}\frac{1}{\hat{c}_1\check{c}_1}+2\frac{ln(\frac{\hat{c}_f}{\check{c}_f})}{\hat{c}_f-\check{c}_f}\frac{ln(\frac{\hat{c}_1}{\check{c}_1})}{\hat{c}_1-\check{c}_1}+ \frac{1}{\hat{c}_f\check{c}_f}\frac{ln(\frac{\hat{c}_1}{\check{c}_1})}{\hat{c}_1-\check{c}_1}(\hat{c}_2+\check{c}_2)+\frac{ln(\frac{\hat{c}_f}{\check{c}_f})}{\hat{c}_f-\check{c}_f}\frac{1}{\hat{c}_1\check{c}_1}(\hat{c}_2+\check{c}_2). \quad (6)$$

The gain FPN is

$$\mathrm{FPN}_{g,lo}=\frac{\sigma_{g,lo}}{\mu_{g,lo}}. \quad (7)$$

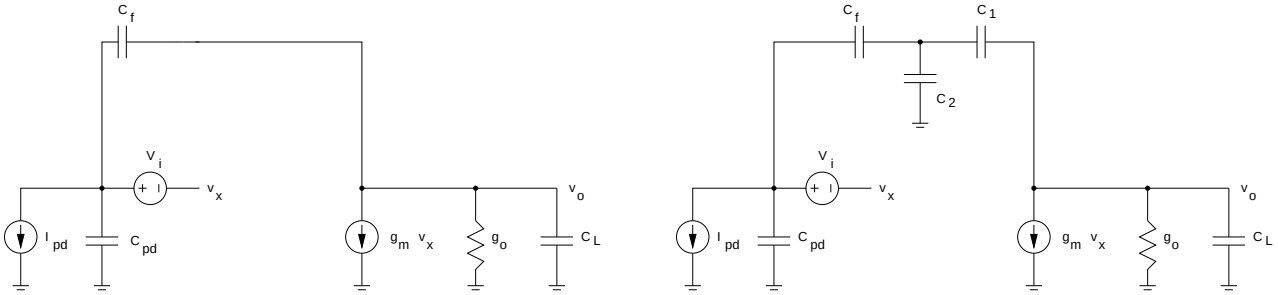

Figure 4. Standard High FPN(left) and High-Gain-Mode LFPN(right) CTIA Small Signal Models

Assuming steady state operation, we use the small signal model in Figure 4 to analyze the gain FPN of a standard high FPN CTIA APS. Let $g_{hi}=\frac{1}{c_f}$. If $\frac{g_m}{g_o} >> c_{pd}g_{hi}+1$, it can be shown that the transimpedance of a standard high FPN CTIA is

$$\frac{v_{o,hi}}{i_{pd}}(s)\approx\left(\frac{1}{s}\right)g_{hi}. \quad (8)$$

Again using the capacitor model discussed above, we find that the mean gain is

$$\mu_{g,hi}=\int g_{hi}p(c_f)dc_f, \quad (9)$$

where $p(c_f)$ is the probability density function of C_f. The expected value squared of the gain is given by

$$\sigma_{g,hi}^2+\mu_{g,hi}^2=\int g_{hi}^2p(c_f)dc_f, \quad (10)$$

and the gain FPN is

$$\mathrm{FPN}_{g,hi}=\frac{\sigma_{g,hi}}{\mu_{g,hi}}=\frac{\sqrt{\frac{(\hat{c}_f-\check{c}_f)^2}{\hat{c}_f\check{c}_f}-ln(\frac{\hat{c}_f}{\check{c}_f})^2}}{ln(\frac{\hat{c}_f}{\check{c}_f})}. \quad (11)$$

Figure 5 illustrates the difference in gain FPN between an LFPN CTIA APS and a standard high FPN CTIA APS when the effective feedback capacitance is varied between 0.1fF and 2fF. Note that in LFPN CTIA APS we used $c_1=20$fF, $c_2=200$fF, and c_f is varied from 1.1fF to 22fF. Although edge effects and oxide thickness variations cause capacitance variations, edge effects typically dominate when the capacitance is small.[10] Therefore the ranges of the uniform random variables in the capacitor model we used to generate Figure 5 are based on the assumption that only variations in the capacitor edge locations affect capacitance variations. In addition, we modeled the capacitors as square metal to metal parallel plate capacitors with 9000Å of silicon oxide between the plates, and a maximum plate to plate misalignment of $\pm0.1\mu$m in both the X and Y directions. Figure 6 shows the relative error of each capacitor as a function of capacitance.

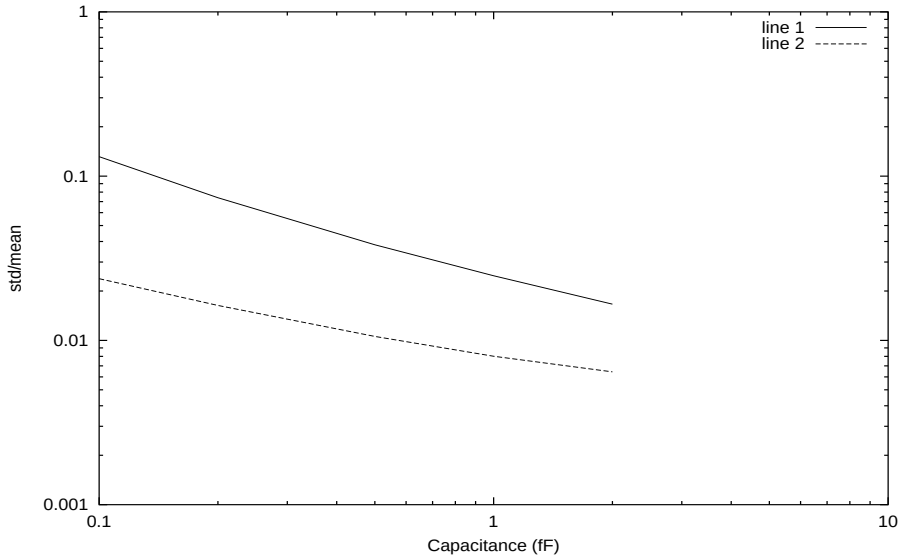

Figure 5. Gain FPN for Standard High FPN(1) and LFPN(2) CTIA APS vs. effective feedback capacitance.

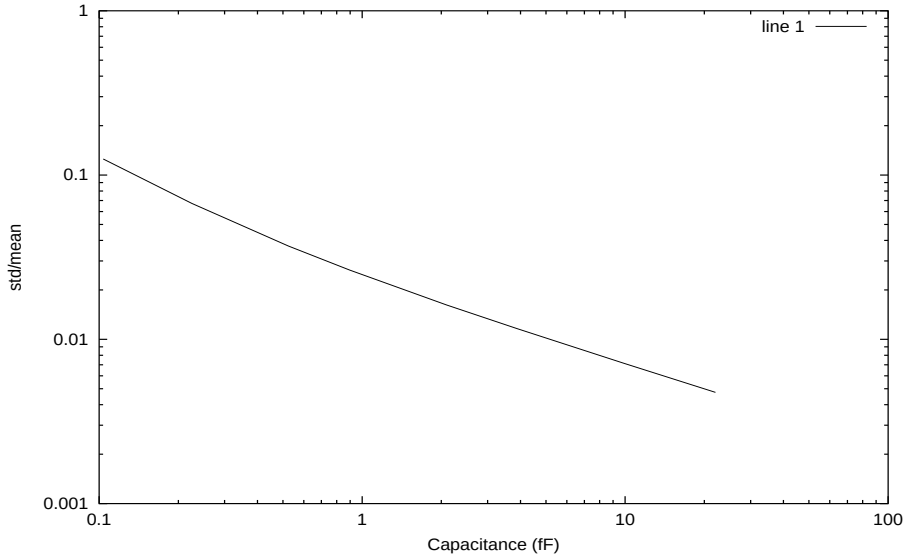

Figure 6. Relative Capacitance Error

2.3. Temporal Noise Analysis

In this section, we will analyze the temporal noise of an LFPN CTIA APS and compare it with the temporal noise of a standard high FPN CTIA APS. This is done to show that reducing the gain FPN does not adversely affect the temporal noise in an LFPN CTIA APS. We use uppercase node voltages and currents to represent random variables and lowercase node voltage and currents to represent deterministic variables.

The temporal read noise of the LFPN CTIA pixel in normal high gain mode is the sum of the reset noise from transistor M1, the thermal noise from amplifier TA1, and the shot noise from the collected photocurrent. The noise due to M2 can be neglected, since M2 turns off before M1 and the DC level across C_2 does not affect the noise performance of the pixel. Since correlated double sampling or active reset[11] can be used to eliminate reset noise, we

will focus on analyzing the thermal noise caused by the transconductance amplifier TA1 and the shot noise from the photodiode.

To simplify analysis, we introduce the following notation: $I_{pd} = i_{pd} + I_n$, where i_{pd} is the photodiode current and I_n is the photodiode noise current; $V_i = v_i + V_{ni}$, where v_i is the input voltage of the transconductance amplifier and V_{ni} is the noise voltage on the input of the transconductance amplifier; $V_o = v_o + V_{no}$, where v_o is the output voltage of the transconductance amplifier and V_{no} is the output noise voltage of the transconductance amplifier; and V_{M2}, the thermal noise of transistor M2. The input-referred two-sided power spectral density of the thermal noise of the transconductance amplifier is given by[12]

$$S_{V_{ni}}(f) = \frac{\alpha 2kT}{g_m} \ (\mathrm{V}^2/\mathrm{Hz}), \tag{12}$$

where α is a constant that depends on the amplifier design, typically between 2/3 and 2, k is Boltzmann's constant, T is absolute temperature, and g_m is the transconductance of the amplifier. The two-sided power spectral density of the shot noise I_n is given by[12]

$$S_{I_n}(f) = q i_{pd} \ (\mathrm{A}^2/\mathrm{Hz}), \tag{13}$$

where q is the charge of an electron.

Assuming the amplifier output is in steady state during read-out, we can analyze the LFPN CTIA temporal noise in normal high gain mode using the small signal model in Figure 4. The output-referred noise of the LFPN CTIA in normal high gain mode is given by

$$\sigma^2_{V_{o,lo}} = \int_{-\infty}^{\infty} \left(S_{V_{ni}}(f) \left| \frac{v_{o,lo}}{v_i}(s) \right|^2 + S_{I_n}(f) \left| \frac{v_{o,lo}}{i_{pd}}(s) \right|^2 \right) df, \tag{14}$$

where $s = 2\pi j f$ and $\frac{v_{o,lo}}{v_i}(s)$ and $\frac{v_{o,lo}}{i_{pd}}(s)$ are given in the appendix. The input-referred noise is

$$\sigma^2_{q_{pd},lo} = \frac{\sigma^2_{V_{o,lo}}}{g^2_{lo}}. \tag{15}$$

If $\frac{g_m}{g_o} >> c_{pd} g_{lo} + 1$, then

$$\sigma^2_{q_{pd},lo} \approx \alpha kT \left(k_2 k_1 \frac{1}{c_l + c_1 \| \| (c_2 + c_f \| \| c_{pd})} \right) + q i_{pd} t_i, \tag{16}$$

where c_l is the load, t_i is the integration time, k_1 and k_2 are in the appendix, and $c_a \| \| c_b$ denotes series capacitors.

The temporal read noise of a standard high FPN CTIA APS is the sum of the reset noise from transistor M1, the thermal noise from amplifier TA1, and the shot noise from the collected photocurrent. Since correlated double sampling or active reset can be used to eliminate the reset noise, we will focus on analyzing the thermal noise caused by the transconductance amplifier TA1 and the shot noise from the photodiode.

Assuming the amplifier output is in steady state during read-out, we analyze the standard high FPN CTIA pixel noise using the small signal model in Figure 4. Output-referred noise of a standard high FPN CTIA is given by

$$\sigma^2_{V_{o,hi}} = \int_{-\infty}^{\infty} \left(S_{V_{ni}}(f) \left| \frac{v_{o,hi}}{v_i}(s) \right|^2 + S_{I_n}(f) \left| \frac{v_{o,hi}}{i_{pd}}(s) \right|^2 \right) df, \tag{17}$$

where $\frac{v_{o,hi}}{v_i}(s)$ and $\frac{v_{o,hi}}{i_{pd}}(s)$ are given in the appendix. The input-referred noise is

$$\sigma^2_{q_{pd},hi} = \frac{\sigma^2_{V_{o,hi}}}{g^2_{hi}}, \tag{18}$$

and if $\frac{g_m}{g_o} >> c_{pd} g_{hi} + 1$, then

$$\sigma^2_{q_{pd},hi} \approx \alpha kT \left(c_f (c_f + c_{pd}) \frac{1}{c_l + c_f \| \| c_{pd}} \right) + q i_{pd} t_i. \tag{19}$$

This result closely agrees with work by Kosonocky[13] and Kozlowski.[14]

Using values of $c_{pd} = 120$fF, $c_f = 22$fF, $c_1 = 20$fF, $c_2 = 200$fF, $c_l = 10$pF, $\frac{g_m}{g_o} > 10000$, $T = 300$K, $\alpha = 1.5$, and $i_{pd} = 0$, the LFPN CTIA APS temporal noise is $\sigma^2_{q_{pd},lo}$ =1.586e-37 C^2 or 2.49 electrons RMS. For a standard high FPN CTIA APS using values of $c_{pd} = 120$fF, $c_f = 2$fF, $c_l = 10$pF, $\frac{g_m}{g_o} > 10000$, $T = 300$K, and $i_{pd} = 0$, the temporal noise is $\sigma^2_{q_{pd},hi}$ =1.522e-37 C^2 or 2.43 electrons RMS. With equivalent feedback capacitances and equivalent gains, an LFPN CTIA APS and a standard high FPN CTIA APS clearly have comparable temporal noise.

3. SIMULATION

We will check the preceeding theoretical results against simulated results using a more elaborate and realistic capacitance model in this section. Figure 7 shows a schematic of the 0.35μm LFPN CTIA APS pixel used for simulation. This circuit uses a 3.3V power supply and draws 2μA of current. Monte Carlo simulation was used to estimate the gain FPN and SPICE was used to estimate the temporal noise. Monte Carlo simulation was performed with 1024 iterations. SPICE simulation used BSIM3 level 3 MOS transistor models with flicker noise coefficients set to zero.

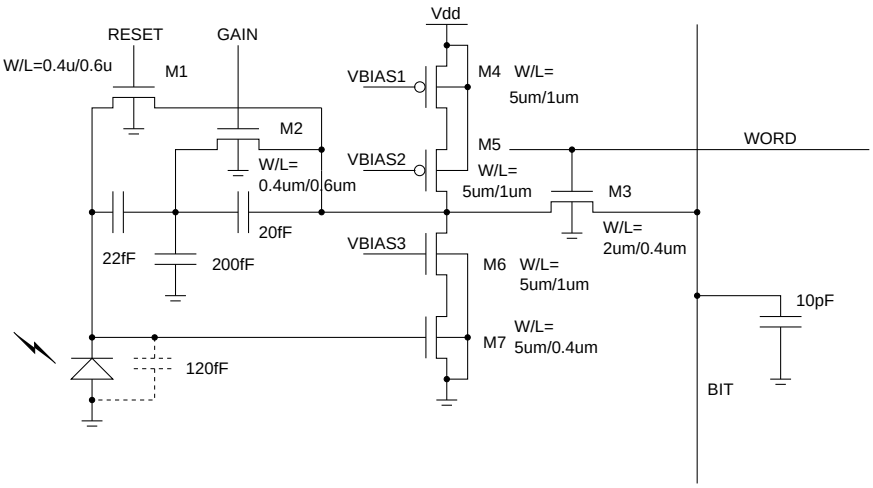

Figure 7. 0.35μm CMOS LFPN CTIA Simulation Circuit

In the previous section, we assumed that the distribution of each capacitance is uniform. In this section, we will use a more realistic model that assumes variation in capacitor length, width, and oxide and metal thickness are uniformly distributed; i.e.,

$$C = \frac{\epsilon_{ox}}{d_{ox} + D_{ox}}(w + W)(l + L) + \frac{1.2\epsilon_{ox}}{\cosh^{-1}(\frac{d_{ox}+D_{ox}+d_{m2}+D_{m2}}{d_{m2}+D_{m2}})}(w + W + l + L), \tag{20}$$

where ϵ_{ox} is the electric permitivity of silicon dioxide, d_{ox} is the M1 to M2 oxide thickness, D_{ox} is the variation in M1 to M2 oxide thickness, d_m is the metal thickness, D_m is the variation in metal thickness, w is the width of the capacitor, W is the variation in width of the capacitor, l is the length of the capacitor, and L is the variation in length of the capacitor. D_{ox}, D_{m2}, W, and L are independent uniform random variables. D_{ox} has a variation of $\pm$50Å, D_{m2} has a variation of $\pm$20Å, W has a variation of $\pm 0.1\mu$m, and L has a variation of $\pm 0.1\mu$m. M1 to M2 oxide thickness d_{ox} is assumed to be 9000Å, and metal thickness is assumed to be 7500Å. c_1, c_2, and c_f were modeled as square M1 to M2 parallel plate capacitors. The edge element of (20) is based on a parallel cylinder model. c_f was varied to achieve an effective feedback capacitance between 0.1fF and 2fF.

Since the area element of this formula is heavily dependent on oxide thickness, the advantages of capacitive voltage divider feedback will start to diminish with higher oxide thickness variation. Although the oxide thickness may vary by 300Å across the wafer and across process variations, we expect it to vary by less than 50Å in any one particular sensor die.

Figure 8 shows Monte Carlo simulation results versus theoretical results. Note that, as the effective feedback capacitance is increased and becomes more dominated by area capacitance, the simulated and theoretical results converge near the upper value shown. For this range of c_f and with oxide thickness variation assumed not to exceed $\pm$50Å across the sensor, the theoretical results upper bound the simulated values. Finally, output-referred temporal noise using SPICE was 235μV RMS. Since the effective feedback capacitance is 2fF, the input-referred noise is 2.94 electrons RMS.

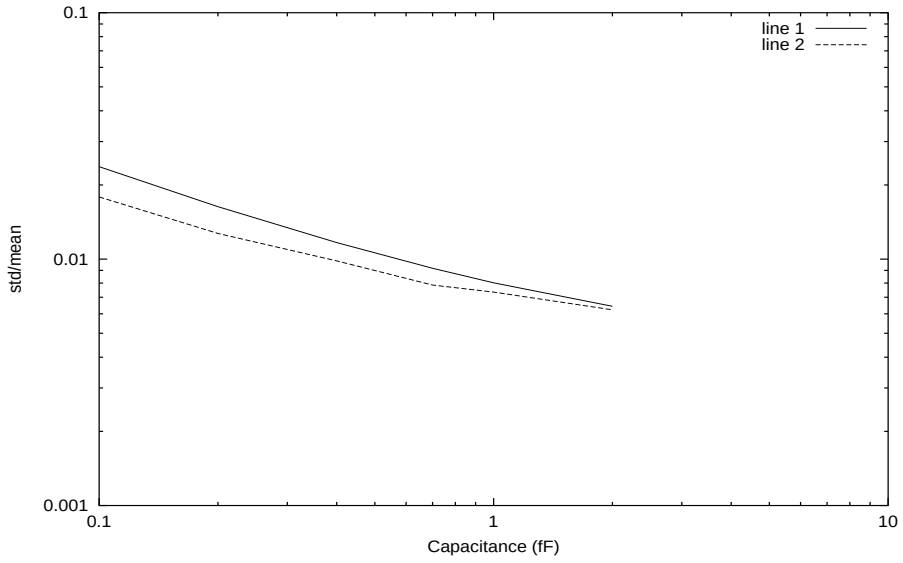

Figure 8. Theoretical(1) and simulated(2) gain FPN for LFPN CTIA APS.

4. DISCUSSION

Table 1 compares theory to simulated results for both the gain FPN and the temporal noise of the circuit in Figure 7. Theory and simulated results show close correlation.

	Theory	Simulation
Gain FPN	0.0064	0.0062
$\frac{\sigma_{q_{pd}}}{q}$	2.49 electrons RMS	2.94 electrons RMS

Table 1. LFPN CTIA APS pixel comparison of theory and simulation.

In addition to low gain FPN and low temporal noise, an LFPN CTIA's switchable gain can be used to increase the sensor's dynamic range. If each pixel in an array had one bit of memory to store pixel gain selection, the sensor could have an impressive effective dynamic range of approximately (1.5V $\times$ 22fF) / (1.6e-19C $\times$ 3 electrons RMS) $\approx$ 68750 = 96.7dB. This assumes that we know the approximate intensity at each pixel and we adjust the gain accordingly. This assumption is poor for video, but quite good for still images.

Due to large pixel-level amplification, the temporal noise in CTIA-based image sensors is almost independent of the read-out speed. For example, our typical 0.35μm CMOS analog output multiplexers operate at about 16Mpixel/sec with 50-70μV RMS noise. This increases the input-referred noise of the sensor by only 0.2 electrons RMS.

5. CONCLUSION

We have shown that an LFPN CTIA APS can be used to achieve low gain FPN when very high pixel sensitivities are required. In addition, we have shown an LFPN CTIA APS does not significantly increase the temporal noise compared against a standard high FPN CTIA APS with equivalent feedback capacitance.

An LFPN CTIA requires additional pixel circuitry. In the implementation discussed in Section 3, one additional transistor and two additional capacitors are required per pixel when compared with a standard high FPN CTIA APS. Consequently, the reduction in gain FPN of an LFPN CTIA APS comes with the price of a larger pixel or a reduced fill factor, if used in an area image sensor. Therefore, an LFPN CTIA APS is best suited for linear or stacked image sensors in which additional pixel circuitry does not affect pixel arrangement.

ACKNOWLEDGEMENTS

We wish to thank Steve Mims, John Lowes, and John Canfield for their helpful comments.

APPENDIX A. CONSTANTS AND EQUATIONS

$$k_1 = c_{pd} + (c_1 + c_2) \| \| c_f \tag{21}$$

$$k_2 = \frac{c_f c_1}{c_1 + c_2 + c_f} \tag{22}$$

$$d_{lo}(s) = g_o + g_m \frac{k_2}{k_1} + (c_l + c_1 \| \| (c_2 + c_f \| \| c_{pd}))s \tag{23}$$

$$\frac{v_{o,lo}}{i_{pd}}(s) = \frac{g_m - k_2 s}{k_1 s} \frac{1}{d_{lo}(s)} \tag{24}$$

$$\frac{v_{o,lo}}{v_i}(s) = \frac{-g_m}{d_{lo}(s)} \tag{25}$$

$$d_{hi}(s) = g_o + g_m \frac{c_f}{c_f + c_{pd}} + (c_l + c_f \| \| c_{pd})s \tag{26}$$

$$\frac{v_{o,hi}}{i_{pd}}(s) = \frac{g_m - c_f s}{(c_f + c_{pd})s} \frac{1}{d_{hi}(s)} \tag{27}$$

$$\frac{v_{o,hi}}{v_i}(s) = \frac{-g_m}{d_{hi}(s)} \tag{28}$$

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